(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 February 2004 (05.02.2004)

PCT

(10) International Publication Number
WO 2004/011999 A1

(51) International Patent Classification[7]: G02F 1/136

(21) International Application Number:
PCT/KR2002/001760

(22) International Filing Date:
18 September 2002 (18.09.2002)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:
2002/0044940 30 July 2002 (30.07.2002) KR

(71) Applicant (*for all designated States except US*): SAMSUNG ELECTRONICS CO., LTD. [KR/KR]; 416, Maetan-dong, Paldal-ku, 442-370 Suwon-city, Kyungki-do (KR).

(72) Inventor; and

(75) Inventor/Applicant (*for US only*): KIM, Dong-Gyu [KR/KR]; 523-1305, Poongdukcheon-ri 1167, Suji-eup, 449-846 Yongin-city, Kyungki-do (KR).

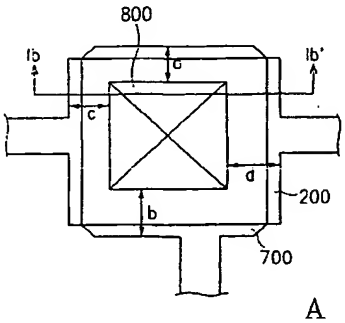
(74) Agent: YOU ME PATENT & LAW FIRM; Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, 135-080 Seoul (KR).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

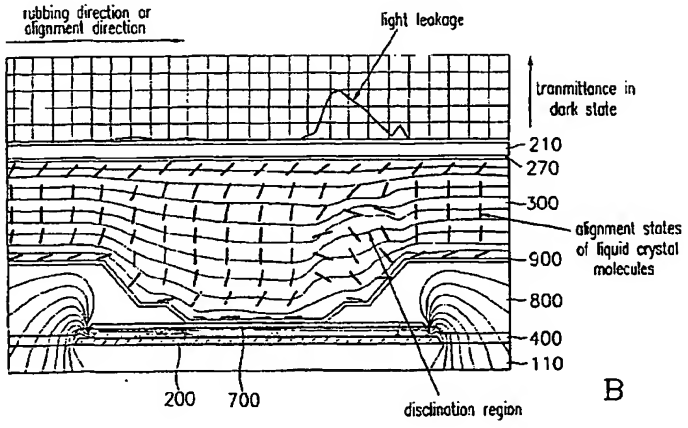
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: THIN FILM TRANSISTOR ARRAY PANEL



A



B

(57) Abstract: A thin film transistor array panel according to the present invention includes a first wire, a second wire, and a pixel electrode. The first wire is formed on an insulating substrate and is used as a gate line or a storage capacitor electrode. The second wire overlaps the first wire via a gate insulating layer and is used as a storage capacitor conductor or a drain electrode. The pixel electrode is formed on a passivation layer covering the second wire and is connected to the second wire through a contact hole of a second insulating layer. In order to secure aperture ratio of the pixel and to block light leakage, distances between the boundaries of the contact hole at the place where alignment treatment or rubbing ends and the boundaries of the first wire or the second wire adjacent thereto and located outside the boundaries of the contact hole are designed to be wider than those between the boundaries of the contact hole at the other places and the boundaries of the first wire or the second wire.

WO 2004/011999 A1